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jc682 U.S. PTO

**UTILITY PATENT APPLICATION TRANSMITTAL
(Large Entity)***(Only for new nonprovisional applications under 37 CFR 1.53(b))*Docket No.
11675.168.1Total Pages in this Submission
3**TO THE ASSISTANT COMMISSIONER FOR PATENTS**Box Patent Application
Washington, D.C. 20231

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

SYSTEM FOR TESTING A SEMICONDUCTOR DEVICE

jc511 U.S. PTO

09/501033

02/09/00

and invented by:

Leonard E. Mess

If a **CONTINUATION APPLICATION**, check appropriate box and supply the requisite information:☐ Continuation ☒ Divisional ☐ Continuation-in-part (CIP) of prior application No.: 09/123,633

Which is a:

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No.:

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Enclosed are:

Application Elements

1. ☒ Filing fee as calculated and transmitted as described below
2. ☒ Specification having Thirty-one (31) pages and including the following:
 - a. ☒ Descriptive Title of the Invention
 - b. ☒ Cross References to Related Applications *(if applicable)*
 - c. ☐ Statement Regarding Federally-sponsored Research/Development *(if applicable)*
 - d. ☐ Reference to Microfiche Appendix *(if applicable)*
 - e. ☒ Background of the Invention
 - f. ☒ Brief Summary of the Invention
 - g. ☒ Brief Description of the Drawings *(if drawings filed)*
 - h. ☒ Detailed Description
 - i. ☒ Claim(s) as Classified Below
 - j. ☒ Abstract of the Disclosure

UTILITY PATENT APPLICATION TRANSMITTAL (Large Entity)

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Docket No.
11675.168.1

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3

Application Elements (Continued)

3. ☒ Drawing(s) (when necessary as prescribed by 35 USC 113)
- a. ☒ Formal Number of Sheets Four (4)
- b. ☐ Informal Number of Sheets _____
4. ☒ Oath or Declaration
- a. ☐ Newly executed (original or copy) ☐ Unexecuted
- b. ☒ Copy from a prior application (37 CFR 1.63(d)) (for continuation/divisional application only)
- c. ☒ With Power of Attorney ☐ Without Power of Attorney
- d. ☐ DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application,
see 37 C.F.R. 1.63(d)(2) and 1.33(b).
5. ☒ Incorporation By Reference (usable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. ☐ Computer Program in Microfiche (Appendix)
7. ☐ Nucleotide and/or Amino Acid Sequence Submission (if applicable, all must be included)
- a. ☐ Paper Copy
- b. ☐ Computer Readable Copy (identical to computer copy)
- c. ☐ Statement Verifying Identical Paper and Computer Readable Copy

Accompanying Application Parts

8. ☒ Assignment Papers (cover sheet & document(s))
9. ☐ 37 CFR 3.73(B) Statement (when there is an assignee)
10. ☐ English Translation Document (if applicable)
11. ☐ Information Disclosure Statement/PTO-1449 ☐ Copies of IDS Citations
12. ☐ Preliminary Amendment
13. ☒ Acknowledgment postcard
14. ☒ Certificate of Mailing
- ☐ First Class ☒ Express Mail (Specify Label No.): EL446924158US

UTILITY PATENT APPLICATION TRANSMITTAL
(Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No.
11675.168.1

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3

Accompanying Application Parts (Continued)

15. ☐ Certified Copy of Priority Document(s) (if foreign priority is claimed)
16. ☒ Additional Enclosures (please identify below):

Associate Power of Attorney
PrintEFS Form

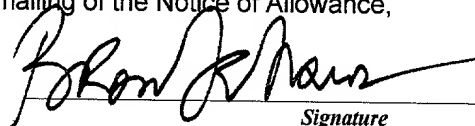
Fee Calculation and Transmittal

CLAIMS AS FILED

For	#Filed	#Allowed	#Extra	Rate	Fee
Total Claims	60	- 20 =	40	x \$18.00	\$720.00
Indep. Claims	8	- 3 =	5	x \$78.00	\$390.00
Multiple Dependent Claims (check if applicable) <input type="checkbox"/>					\$0.00
BASIC FEE					\$760.00
OTHER FEE (specify purpose)					\$0.00
TOTAL FILING FEE					\$1,870.00

- ☒ A check in the amount of \$1,870.00 to cover the filing fee is enclosed.
- ☒ The Commissioner is hereby authorized to charge and credit Deposit Account No. 23-3178 as described below. A duplicate copy of this sheet is enclosed.
- ☐ Charge the amount of _____ as filing fee.
- ☒ Credit any overpayment.
- ☒ Charge any additional filing fees required under 37 C.F.R. 1.16 and 1.17.
- ☐ Charge the issue fee set in 37 C.F.R. 1.18 at the mailing of the Notice of Allowance, pursuant to 37 C.F.R. 1.311(b).

Dated: February 9th, 2000



Signature

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Docket No.

11675.168.1

Serial No.

Not Yet Assigned

Filing Date

February 9, 2000

Examiner

Not Yet Assigned

Group Art Unit

Not Yet Assigned

Invention: **SYSTEM FOR TESTING A SEMICONDUCTOR DEVICE**

I hereby certify that this **Divisional Patent Application and other related documents ***
(Identify type of correspondence)

is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under
37 CFR 1.10 in an envelope addressed to: The Assistant Commissioner for Patents, Washington, D.C. 20231 on
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Note: Each paper must have its own certificate of mailing.

* Transmitted: Divisional Patent Application (31 pgs)
Formal Drawings (4 pgs)
Copy of Declaration, Power of Attorney, and Petition (3 pgs)
Copy of Assignment (3 pgs)
Associate Power of Attorney (2 pgs)
PrintEFS Form (2 pgs)
Transmittal Letter (3 pgs)
Certificate of Express Mail Label No. EL446924158US (1 pg)
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CORRESPONDENCE INFORMATION

APPLICATION INFORMATION

REPRESENTATIVE INFORMATION

CONTINUITY INFORMATION

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This application is a::      DIVISION OF
> Application One::         09/123,633
  Filing Date::            07-28-1998

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PATENT APPLICATION
Docket No. 11675.168.1

of

LEONARD E. MESS

for

SYSTEM FOR TESTING A SEMICONDUCTOR DEVICE

WORKMAN, NYDEGGER & SEELEY

A PROFESSIONAL CORPORATION
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[illegible]

1 1. Related Applications.

2 This is a divisional application of US Patent Application Serial No. 09/123,633,
3 filed on July 28, 1998, titled "THERMALLY CONDUCTIVE INTERPOSER AND
4 METHOD" which is incorporated herein by reference.

5
6 **BACKGROUND OF THE INVENTION**

7 2. **The Field of the Invention**

8 This invention is in the field of semiconductive device technology. More
9 specifically, this invention is in the field of interposers for electrically connecting
10 semiconductive devices to an electrical apparatus.

11
12 3. **The Relevant Technology**

13 A semiconductive device is often electrically coupled to an electrical apparatus such
14 as a computer through the use of an interposer. In one such process, the semiconductive
15 device is connected to the interposer, which is then inserted into the socket of the electrical
16 apparatus. The socket may be mounted on the motherboard of a computer, for example.
17 Thus, the semiconductive device communicates electrically through the interposer with the
18 electrical apparatus. Typical interposers currently employed in the coupling of
19 semiconductive devices to electrical apparatuses are comprised of an FR4 fiberglass material,
20 or the like, having electrically conductive metal lines or traces thereon.

21 The term "semiconductive device" extends to any device or assembly that includes
22 circuitry defined in a semiconductive material, and further extends to a chip package that
23 includes semiconductive material. The external and additional structure of a package
24 assembly may be used, for example, for mounting the semiconductive device to a printed
25 circuit board or other external circuitry, for establishing electrical connection between the
26 semiconductive device and external circuitry, for improving the ease of handling or

transporting the semiconductive device, and/or for protecting the semiconductive device from environmental conditions. Many chip packages include a lead frame that extends beyond the body thereof. The lead frame typically includes an array of electrical leads that extend from the internal circuitry of the integrated circuit to the exterior portion of the chip package where they are exposed to the surroundings.

Frequently, after a semiconductive device is manufactured, a testing process is conducted on the semiconductive device by subjecting it to a preselected set of input conditions in order to measure its response or other parameters. Testing of an integrated circuit package that includes a lead frame assembly is conventionally conducted by providing temporary electrical communication between the leads and testing circuitry. For example, such temporary electrical connection may be established by using a set of probes, pins, sockets, or the like, to contact the leads. The integrated circuit package may be clamped or otherwise secured in position during the testing operation in order for the leads to remain in electrical contact with the corresponding probes, pins, sockets, etc., of the testing circuitry.

Semiconductive devices, such as DRAMs and SRAMs, undergo significant stresses when in use. Particularly modern, high speed, advanced-integration semiconductive devices generate a significant amount of heat during use. This heat can degrade and slow down semiconductive devices. For example, testing of semiconductive devices to determine the quality and capability of the devices can generate such heat within the devices that the testing process itself damages the devices. Typical fiberglass interposers do not dissipate heat sufficient to protect semiconductive devices from the potential of damage caused by the heat generated during use of the device.

In addition, typical fiberglass interposers are made of glass fibers and epoxy resin. The resulting interposer has a coefficient of thermal expansion which is incompatible with typical semiconductive devices. The coefficient of thermal expansion of the fiberglass is often significantly greater than that of the semiconductive device.

As a result of this thermal expansion incompatibility, shear stresses develop in the interface between the interposer and the semiconductive device when the semiconductive device becomes hot. These shear stresses can result in a severing of the electrical connection between the interposer and the semiconductive device. While it is possible to ameliorate the effects of shearing through a process known as wire bonding, this process adds additional complexity and expense. Furthermore, the organic material within FR4 fiberglass interposers absorbs moisture, causing the interposers to degrade.

8 There is therefore a need in the art for an improved interposer which assists in
9 protecting a semiconductive device coupled to the interposer from the potential damage
10 caused by significant amounts of heat generated by the semiconductive device. There is also
11 a need in the art for an improved interposer which prevents shear stress from severing the
12 electrical connection between the interposer and the semiconductive device.

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10 In one embodiment, a thermally conductive connector connects the semiconductive
11 device, such as an SRAM, DRAM, or integrated circuit device, to the interposer such that
12 a portion of the semiconductive device is exposed to the atmosphere to thereby dissipate heat
13 to the atmosphere. Both the thermally conductive interposer and the thermally conductive
14 connector act as heat sinks to conduct heat from the semiconductive device to the ambient,
15 thereby protecting the semiconductive device from overheating. The interposer preferably
16 has a coefficient of thermal expansion which is substantially similar to the coefficient of
17 thermal expansion of a semiconductive device on the interposer, thereby preventing shearing
18 of the electrical connection between the semiconductive device and the interposer.

Docket No. 11675.168.1

1 These and other features of the present invention will become more fully apparent
2 from the following description and appended claims, or may be learned by the practice of the
3 invention as set forth hereinafter.

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DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

With reference now to Figures 1 and 2, the present invention relates to an interposer system 10 comprising (i) an interposer 12; and (ii) a connector 14 for connecting a semiconductor device 16 to interposer 12. Interposer 12 is configured to electrically couple semiconductor device 16 to an electrical apparatus (not shown in Fig. 1), such as a testing apparatus which monitors, tests or evaluates device 16, by for example storing information on device 16 and retrieving information from device 16.

Interposer 12 is electrically coupled to the electrical connections 17 of device 16, the bottom surface of which is shown in Figure 2, and to electrical connections on an electrical apparatus, thereby electrically coupling semiconductor device 16 to the electrical apparatus. By coupling semiconductor devices 16 on interposer 12, and coupling interposer 12 to the electrical apparatus, the electrical apparatus may perform a variety of functions upon the semiconductor devices, while the semiconductor devices are protected from overheating by the heat dissipating qualities of interposer 12.

Interposer 12 and preferably, connector 14, are thermally conductive. As shown in Figure 1, system 10 preferably exposes semiconductor device 16 partially to the open atmosphere, rather than completely covering devices 16 with a connector, allowing heat to dissipate to the atmosphere directly from semiconductor device 16. In addition, heat is transferred through thermally conductive interposer 12 and connector 14 from semiconductor device 16, then dissipated to the atmosphere. The thermal conductivity of interposer 12 and connector 14, along with the configuration of interposer 12 and connector 14 are significant advantages within the art.

Interposer 12 will now be discussed in additional detail. Interposer 12 is comprised of a substrate 18 and a plurality of electrical conductors 20 on substrate 18. Substrate 18 is comprised of an electrically insulating material. Substrate 18 also conducts heat, thereby dissipating heat away from device 16 connected to substrate 18. When exposed to the high

In addition to glass, other ceramics useful in the present invention as substrate 18 include alumina, aluminum nitrides, nonmetallic nitrides, nonmetallic carbides, single oxide ceramics, mixed oxide ceramics, and mixtures and derivatives thereof. As used throughout this specification and the appended claims, the term "nonmetallic nitrides" includes boron nitrides, silicon nitrides and other transitional element nitrides. Alumina, for example, may be used alone or in combination with silica or silicates, for example, because alumina resists harsh environments and also dissipates heat.

1 Other examples of ceramics useful in the present invention for substrate 18 include
2 glass ceramics, such as nucleated glass having a nonporous, substantially crystalline
3 structure, devitrified ceramics, or vitro ceramics. In one embodiment, glass ceramics are
4 fine-grained substantially crystalline materials made through controlled crystallization from
5 glass compositions containing nucleating agents. Thus, in one embodiment, substrate 18
6 comprises a material selected from the group consisting of glass, alumina, glass ceramic,
7 aluminum nitride, nonmetallic nitride, nonmetallic carbide, and mixtures and derivatives
8 thereof. Other possible, but less preferred ceramics for substrate 18 include refractories such
9 as steatite and mullite.

10 Glass and other ceramics are preferably provided in a substantially homogeneous
11 form for substrate 18, as opposed to the heterogeneous mixture of fibers and epoxy found in
12 FR4 fiberglass. Glass and other ceramics are also preferably provided in substrate 18 in a
13 substantially planar (i.e., flat) sheet, as shown in Figure 1.

14 As shown in Figure 1, interposer 12 includes a plurality of arrays 22, 24, 26 of
15 electrical conductors 20 thereon. Each electrical conductor 20 has a receiving end 28 for
16 connecting to a corresponding terminal 30 of an electrical conductor 32 on the bottom
17 surface of semiconductive device 16 as shown in Figure 2. Each electrical conductor 20 on
18 substrate 18 further comprises a terminal end 34 for connecting to an electrical apparatus.
19 An intermediate portion 36 of conductor 20 extends between receiving end 28 and terminal
20 end 34 of each conductor 20. The connection of terminal end 34 to the electrical apparatus
21 may be permanent or removable.

22 An interposer of the present invention may comprise a single conductor or a plurality
23 of conductors. The interposer may have a single array of conductors or may have a plurality
24 of arrays, such as arrays 22, 24, 26 as shown in Figure 1. Each array may have as many
25 conductors as needed to electrically couple a particular semiconductive device, such as
26 device 16, to an electrical apparatus. Conductors may have a variety of different

With reference now to Figures 3, 4, and 5, various embodiments of biasing connectors are demonstrated. As shown in Figure 3, connector 14 comprises a resilient clip having a top plate 38, a bottom plate 40, and an intermediate portion 42 coupling top plate

1 Connectors 14, 44, 56 dissipate heat because they are in intimate thermal contact
2 with devices 16 and because they are comprised of a thermally conductive material.
3 Connectors 14, 44, 56 and other such connectors may be placed on device 16 manually or
4 automatically. One advantage of such connectors over an underfilling process is that the
5 connectors do not need a delay time in which wicking occurs and they avoid the further delay
6 of repeated applications, as well as delays associated with curing of the adhesive.

7 Connectors 14, 44, 56 or a variety of substantially similar connectors may also be
8 employed to assist in permanently coupling devices 16 to substrate 18, thereby providing
9 heat dissipation. For example, it is possible to employ both an adhesive, such as a thermally
10 conductive adhesive and a connector, such as connector 14, 44, or 56 to permanently couple
11 semiconductive device 16 to interposer 12. This may be accomplished, for example, by
12 placing adhesive between substrate 18 and semiconductive device 16 with a connector 14,
13 44, or 56 to couple both substrate 18 and device 16 together and/or by placing the adhesive
14 between connector 14, 44, or 56 and substrate 18, for example. Adhesive may also be placed
15 between connector 14, 44, or 56 and device 16 so long as the electrical connections between
16 connector 14, 44, or 56 and device 16 are preserved.

17 Conductors 20 may be conventionally formed on substrate 18 by being attached or
18 deposited thereon. For example, a metal can be sputtered onto substrate 18, followed by a
19 patterning process to define conductors 20. Other conventional metallizing or metal line
20 deposition processes can also be used. In one embodiment, substrate 18 is initially etched,
21 after which the etched portion is metallized, by metal deposition and a metal line patterning
22 process. Metal deposition and photolithographic metallization processes may be used to etch
23 fine line widths and to place conductors in dense arrays on substrates to form interposers.

24 As shown in Figure 6, in one embodiment, electrical conductor 20 has a bumped
25 receiving end 28 which projects from the upper surface of substrate 18. In this embodiment,
26 semiconductive device 16 includes a corresponding electrical conductor 32 having a bumped

1 terminal 30 which couples to receiving end 28, thereby forming a connection between bump
2 30 and bump 28 when device 16 and interposer 12 are connected together such that bumps
3 28 and 30 interface. This creates a physical connection between substrate 18 and device 16.
4 This configuration allows bumps 28, 30 to slide against one another, permitting convenient
5 coupling of bumps 28, 30 together as well as removal of bumps 28, 30 one from another.

6 In another embodiment, as shown in Figure 7, the electrical connection between an
7 interposer 59 and a semiconductive device 58 is created by providing for a complimentary,
8 male/female connection between device 58 and interposer 59. Although interposer 59 is
9 shown as comprising the female fitting, the interposer may comprise the male fitting, as
10 shown in Figure 6 with protruding bumped receiving end 28, while the semiconductive
11 device comprises the female fitting which is formed in a recess of the semiconductive device.

12 In the embodiment shown in Figure 7, interposer 59 comprises a substrate 60 having
13 a recess 62 therein. A conductor 64 such as a metal trace is placed on substrate 60 such that
14 a receiving end 66 of conductor 64 is disposed within recess 62, which is below the upper
15 surface of substrate 60, allowing a male connecting terminal 68 of a conductor on
16 semiconductive device 58 to be electrically coupled with receiving end 66 by being placed
17 therein. Conductor 64 also has a terminal end (not shown) for connecting to an electrical
18 apparatus. A connector such as connector 14, 44, or 56 may then be placed to bias device
19 58 towards substrate 60 to thereby retain the electrical connection between bump 68 and
20 recessed receiving end 66. It will be appreciated that the male/female complimentary fit
21 shown in Figure 7 would be advantageous because of the structural integrity and non-slip
22 design derived therefrom.

23 According to one method of manufacturing interposer 12 or 59, a substrate 18 or 60
24 of the present invention is provided comprising a ceramic material. At least one electrical
25 conductor 20 or 64 is then coupled onto the substrate. In one embodiment, recess 62 is
26 formed within substrate 60, such as through etching, and at least a portion of conductor 64

Apparatus 70 includes a socket, such as a printed circuit board socket, having electrical terminals onto which terminal ends 34 of conductors 20 of interposer 12 are placed. After terminal ends 34 of interposer 12 are placed into the socket, an electrical connection

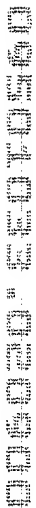
1 exists between semiconductive devices 16 and apparatus 70, thereby allowing a user to test
2 device 16 or otherwise engage in a variety of different functions.

3 Thus, one method for testing semiconductive device comprises providing an
4 interposer having substrate comprised of an electrically insulating, thermally conductive
5 ceramic material, electrically coupling the interposed to a semiconductive device, electrically
6 coupling the interposer to a testing apparatus such that the testing apparatus is electrically
7 coupled to semiconductive device, and then actuating the testing apparatus to electrically
8 communicate with the semiconductive device.

9 A variety of different semiconductive devices may be electrically coupled to the
10 inventive interposer. Examples of such semiconductive devices include DRAMs, SRAMs,
11 integrated circuit devices, and the like, each of which has electrical conductors thereon such
12 as bumps, lead fingers, or other package connections. The semiconductive devices, however,
13 may be either packaged or non-packaged.

14 The present invention may be embodied in other specific forms without departing
15 from its spirit or essential characteristics. The described embodiments are to be considered
16 in all respects only as illustrative and not restrictive. The scope of the invention is, therefore,
17 indicated by the appended claims rather than by the foregoing description. All changes
18 which come within the meaning and range of equivalency of the claims are to be embraced
19 within their scope.

20 What is claimed and desired to be secured by United States Letters Patent is:



- 1 5. A system as recited in claim 1, wherein the connector is composed of a metal
2 material.
3
4 6. A system as recited in claim 1, wherein the connector comprises an adhesive.
5
6 7. A system as recited in claim 1, wherein at least one of said receiving ends
7 projects from the substrate.
8
9 8. A system as recited in claim 1, wherein at least one of said receiving ends is
10 disposed within a recess in the substrate.

1 9. A system for testing a semiconductive device, the system comprising:
2 an electrical testing apparatus;
3 a semiconductive device having an electrical circuitry therein electrically
4 connected to an electrical lead projecting therefrom;
5 an interposer, the interposer comprising:

6 a substrate comprised of an electrically insulating material
7 selected from the group consisting of glass, alumina, glass ceramic,
8 nonmetallic nitride, aluminum nitride, nonmetallic carbide, and
9 mixtures and derivatives thereof; and

10 an electrical conductor on the substrate, the electrical
11 conductor having a receiving end for connecting to the electrical lead
12 of the semiconductive device and a terminal end for connecting to the
13 electrical testing apparatus, whereby the semiconductive device is
14 electrically coupled to the electrical testing apparatus when the
15 electrical lead of the semiconductive device is in contact with the
16 receiving end of the electrical conductor and the terminal end of the
17 electrical conductor is in electrical communication with the electrical
18 testing apparatus.

19
20 10. The system as defined in Claim 9, further comprising:

21 a connector for biasing the electrical lead of the semiconductive device
22 towards and in contact with the receiving end of the electrical conductor, the
23 connector being composed of copper and alloys thereof.

24
25 11. The system as defined in Claim 10, wherein the connector has a coating
26 thereon composed of an electrically insulating material.

1 12. A system as recited in claim 10, wherein the connector connects the
2 semiconductive device to the interposer such that a portion of the semiconductive device is
3 exposed to the atmosphere to thereby dissipate heat to the atmosphere.

4
5 13. A system as recited in claim 10, wherein the connector removably connects
6 the semiconductive device to the interposer.

7
8 14. A system as recited in claim 10, wherein the connector comprises a resilient
9 biasing clip.

10
11 15. A system as recited in claim 10, wherein the connector is composed of a metal
12 material.

13
14 16. A system as recited in claim 10, wherein the connector comprises an adhesive.

15
16 17. A system as recited in claim 9, wherein at least one of said receiving ends
17 projects from the substrate.

18
19 18. A system as recited in claim 9, wherein at least one of said receiving ends is
20 disposed within a recess in the substrate.

1 19. A system for electrically coupling a semiconductive device to an electrical
2 apparatus, the system comprising:

3 an interposer, the interposer comprising:

4 a substrate comprised of an electrically insulating, ceramic material;

5 and

6 an electrical conductor on the substrate, the electrical conductor
7 having a receiving end for connecting to the semiconductive device and a
8 terminal end for connecting to the electrical apparatus; and

9 a connector for holding the semiconductive device stationary relative to the
10 interposer.

11
12 20. The system as defined in claim 19, wherein the substrate comprises a
13 substantially planar sheet.

14
15 21. The system as defined in claim 19, wherein the substrate comprises a
16 substantially homogenous material.

17
18 22. The system as defined in claim 19, wherein the receiving end protrudes
19 upwardly with respect to the substrate.

20
21 23. The system as defined in claim 19 wherein the receiving end is disposed
22 within a recess in the substrate.

23
24 24. The system as defined in claim 19, wherein the substrate comprises a material
25 selected from the group consisting of glass, alumina, glass ceramic, nonmetallic nitride,
26 aluminum nitride, nonmetallic carbide, and mixtures and derivatives thereof.

32. A system as recited in claim 19, wherein the connector comprises an adhesive.

37. The system as recited in claim 35, wherein the substrate consists essentially of a glass ceramic material.

1 38. A system as recited in claim 35, wherein the connector connects the
2 semiconductive device to the interposer such that a portion of the semiconductive device is
3 exposed to the atmosphere to thereby dissipate heat to the atmosphere.

4
5 39. A system as recited in claim 35, wherein the connector performs a function
6 selected from the group consisting of:

7 removably connects the semiconductive device to the interposer;
8 resiliently biases the semiconductive device to the interposer; and
9 adhesively connects the semiconductive device to the interposer.

10
11 40. A system as recited in claim 35, wherein at least one of said receiving ends
12 projects from the substrate.

13
14 41. A system as recited in claim 35, wherein at least one of said receiving ends
15 is disposed within a recess in the substrate.

1 42. A system for electrically coupling a semiconductive device to an electrical
2 apparatus, the system comprising:

3 an interposer, the interposer comprising:

4 a substantially homogeneous, substantially planar sheet composed of
5 an electrically insulating material selected from the group consisting of glass
6 ceramics, devitrified ceramics, vitro ceramics, alumina, single oxide
7 ceramics, and mixed oxide ceramics, and mixtures and derivatives thereof;
8 and

9 an electrical conductor on the sheet, the electrical conductor having
10 a receiving end for connecting to the semiconductive device and a terminal
11 end for connecting to the electrical apparatus, such that the semiconductive
12 device is electrically coupled to the electrical apparatus when the
13 semiconductive device is connected to the receiving end of the electrical
14 conductor and the terminal end of the electrical conductor is connected to the
15 electrical apparatus

16 a connector for holding the semiconductive device stationary relative to the
17 interposer.

18
19 43. A system as recited in claim 42, wherein the connector performs a function
20 selected from the group consisting of:

21 removably connects the semiconductive device to the interposer;
22 resiliently biases the semiconductive device to the interposer; and
23 adhesively connects the semiconductive device to the interposer.
24

25 44. A system as recited in claim 42, wherein at least one of said receiving ends
26 projects from the substrate.

51. A system as recited in claim 47, wherein the connector connects the semiconductive device to the interposer such that a portion of the semiconductive device is exposed to the atmosphere to thereby dissipate heat to the atmosphere.

1 52. A system for electrically coupling a semiconductive device to an electrical
2 apparatus, the system comprising:

3 an interposer, the interposer comprising:

4 a substantially homogeneous, substantially planar sheet composed of
5 an electrically insulating material selected from the group consisting of boron
6 nitrides, aluminum nitrides, and mixtures and derivatives thereof; and

7 an electrical conductor on the sheet, the electrical conductor having
8 a receiving end for connecting to a semiconductive device and a terminal end
9 for connecting to an electrical apparatus, such that the semiconductive device
10 is electrically coupled to the electrical apparatus when the semiconductive
11 device is connected to the receiving end of the electrical conductor and the
12 terminal end of the electrical conductor is connected to the electrical
13 apparatus

14 a connector for holding the semiconductive device stationary relative to the
15 interposer.
16

17 53. A system as recited in claim 52, wherein the connector performs a function
18 selected from the group consisting of:

19 removably connects the semiconductive device to the interposer;
20 resiliently biases the semiconductive device to the interposer; and
21 adhesively connects the semiconductive device to the interposer.
22

23 54. A system as recited in claim 52, wherein at least one of said receiving ends
24 projects from the substrate.
25

1 55. A system as recited in claim 52, wherein at least one of said receiving ends
2 is disposed within a recess in the substrate.

3
4 56. A system as recited in claim 52, wherein the connector connects the
5 semiconductive device to the interposer such that a portion of the semiconductive device is
6 exposed to the atmosphere to thereby dissipate heat to the atmosphere.

7
8 57. A system for electrically coupling a semiconductive device to an electrical
9 apparatus, the system comprising:

10 an interposer, the interposer comprising:

11 a substantially homogeneous, substantially planar sheet composed of
12 an electrically insulating material selected from the group consisting of
13 oxides of silicon, silicate glass, and nucleated, substantially crystalline glass,
14 and mixtures and derivatives thereof; and

15 an electrical conductor on the sheet, the electrical conductor having
16 a receiving end for connecting to the semiconductive device and a terminal
17 end for connecting to the electrical apparatus, such that the semiconductive
18 device is electrically coupled to the electrical apparatus when the
19 semiconductive device is connected to the receiving end of the electrical
20 conductor and the terminal end of the electrical conductor is connected to the
21 electrical apparatus

22 a connector for holding the semiconductive device stationary relative to the
23 interposer.

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removably connects the semiconductive device to the interposer;
resiliently biases the semiconductive device to the interposer; and
adhesively connects the semiconductive device to the interposer.

59. A system as recited in claim 57, wherein at least one of said receiving ends projects from the substrate.

10 60. A system as recited in claim 57, wherein at least one of said receiving ends
11 is disposed within a recess in the substrate.

61. A system as recited in claim 57, wherein the connector connects the
semiconductive device to the interposer such that a portion of the semiconductive device is
exposed to the atmosphere to thereby dissipate heat to the atmosphere.

A system including an interposer and a coupler for electrically coupling a semiconductor device to an electrical apparatus. The system also includes (i) a substrate comprised of an electrically insulating, thermally conductive ceramic material; and (ii) an electrical conductor on the substrate having a receiving end for connecting to a semiconductor device and a terminal end for connecting to an electrical apparatus. The semiconductor device is electrically coupled to the electrical apparatus when the semiconductor device is connected to the receiving end of the electrical conductor and the terminal end of the electrical conductor is connected to the electrical apparatus. A thermally conductive coupler or connector connects the semiconductor device to the interposer. The thermally conductive interposer and connector conduct heat from the semiconductor device to the environment, thereby protecting the semiconductor device from overheating.

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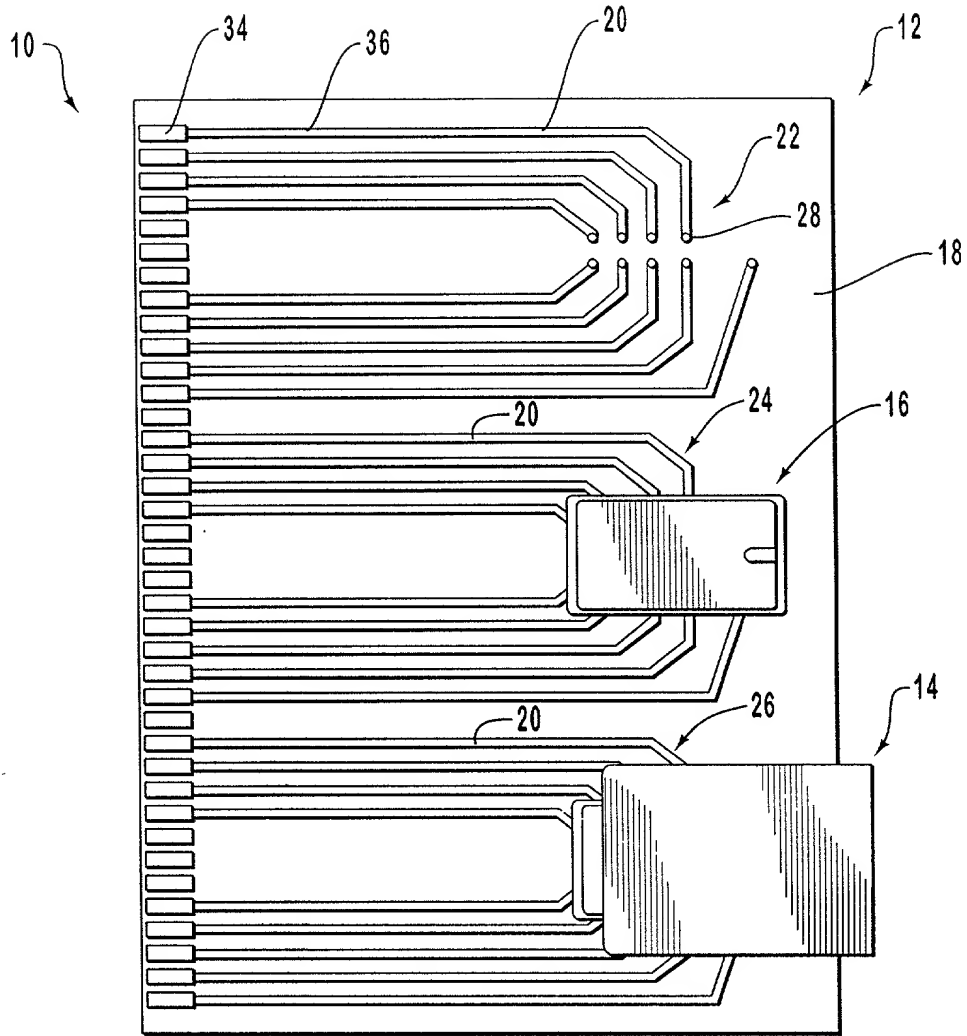


FIG. 1

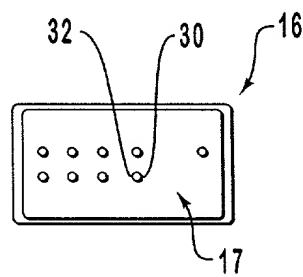


FIG. 2

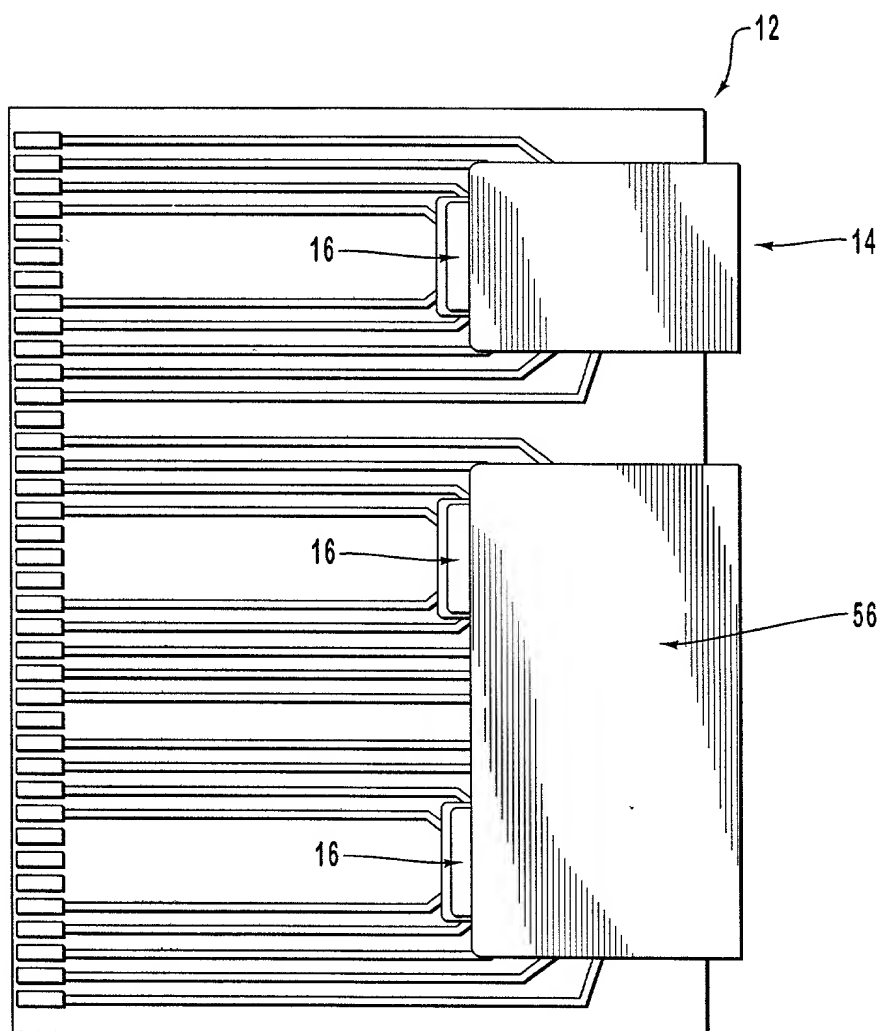
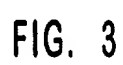
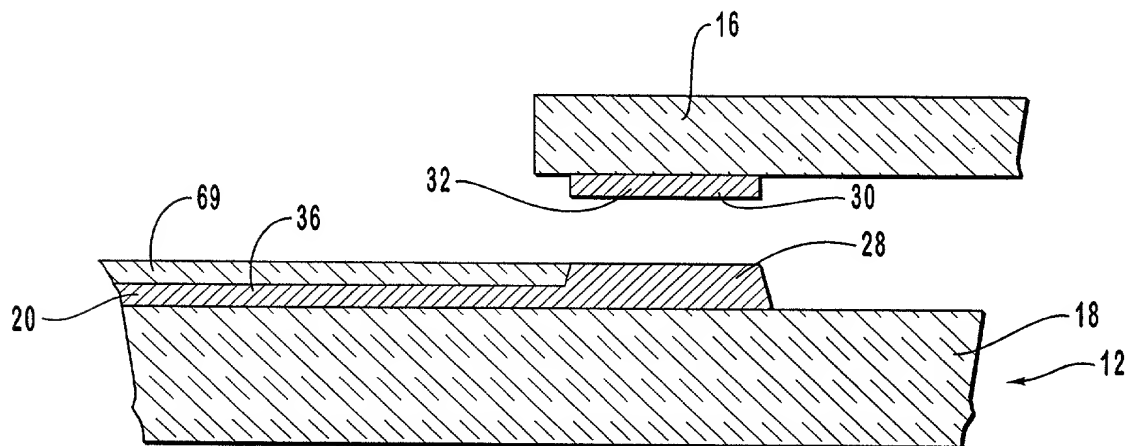
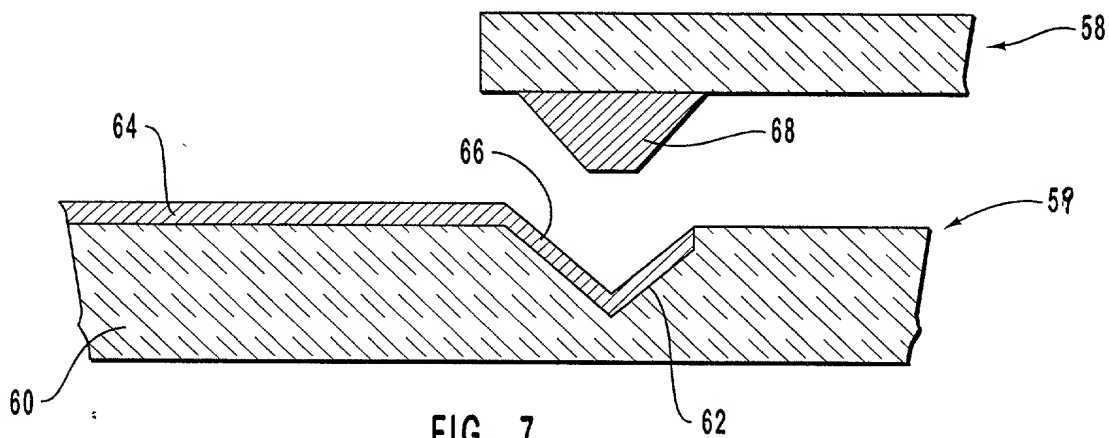
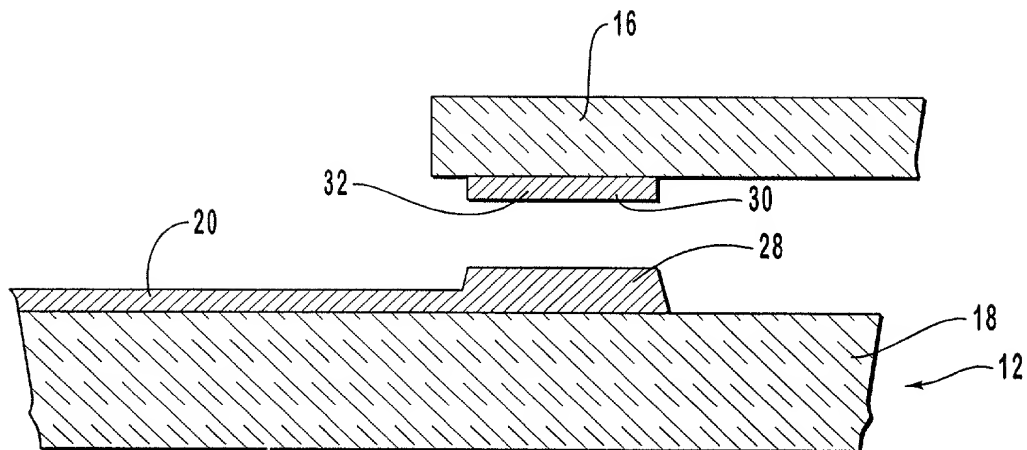
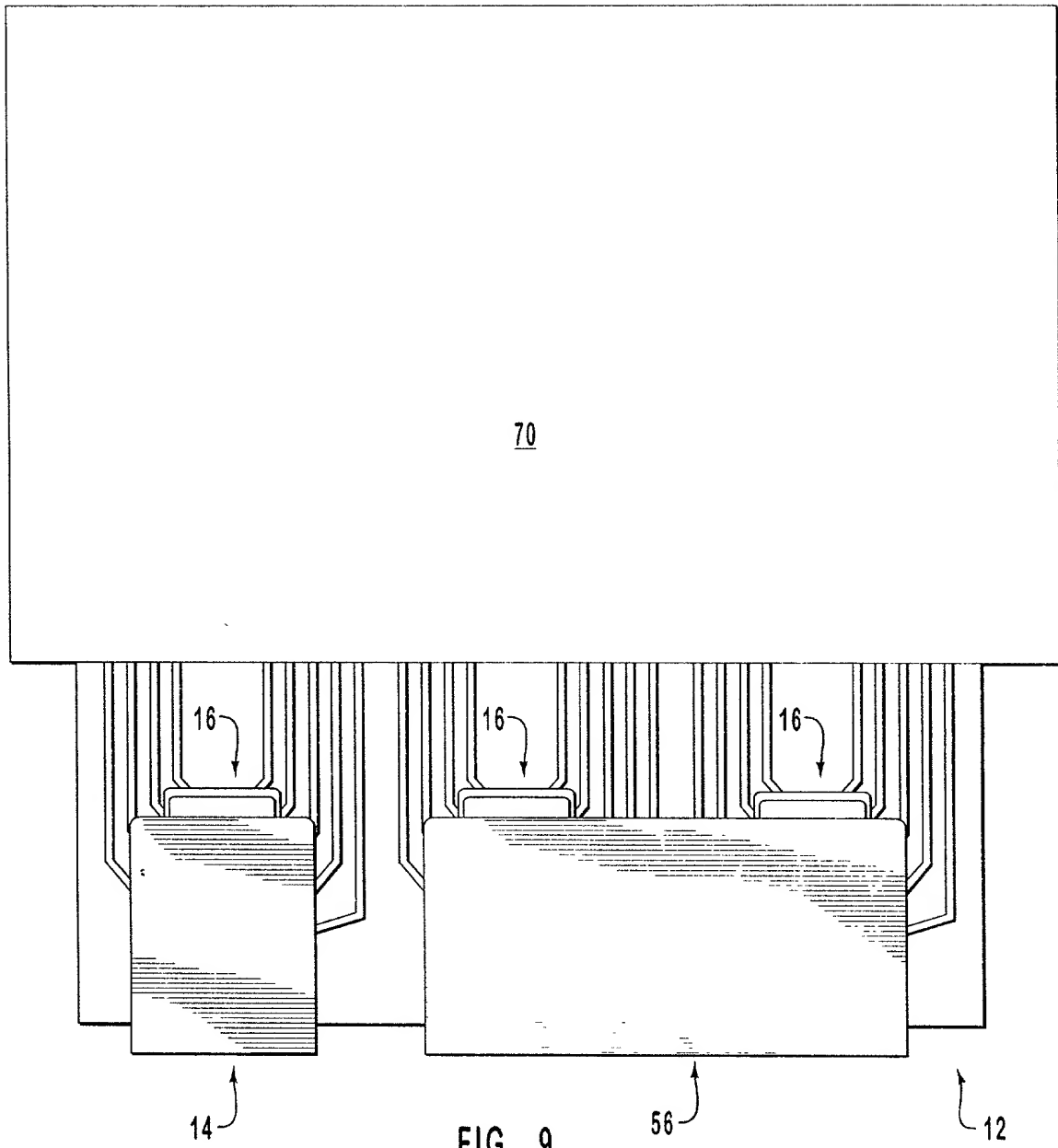


FIG. 5





DECLARATION, POWER OF ATTORNEY, AND PETITION

I, Leonard E. Mess, declare: that I am a citizen of the United States of America; that my residence and post office address is 4101 Cassia, Boise, Idaho 83705; that I verily believe I am the original, first, and sole inventor of the subject matter of the invention or discovery entitled THERMALLY CONDUCTIVE INTERPOSER AND METHOD OF USE, for which a patent is sought and which is described and claimed in the specification attached hereto; that I have reviewed and understand the contents of the above-identified specification, including the claims; and that I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Section 1.56(a) of Title 37 of the Code of Federal Regulations.

I declare further that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful, false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful, false statements may jeopardize the validity of the application or any patent issuing thereon.

I hereby appoint as my attorneys and/or patent agents: RICK D. NYDEGGER, Registration No. 28,651; DAVID O. SEELEY, Registration No. 30,148; JONATHAN W. RICHARDS, Registration No. 29,843; JOHN C. STRINGHAM, Registration No. 40,831; MICHAEL F. KRIEGER, Registration No. 35,232; BRADLEY K. DeSANDRO, Registration No. 34,521; JOHN M. GUYNN, Registration No. 36,153; GREGORY M. TAYLOR, Registration No. 34,263; DANA L. TANGREN, Registration No. 37,246; ERIC L. MASCHOFF, Registration No. 36,596; KEVIN

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All correspondence and telephonic communications should be directed to:

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Wherefore, I pray that Letters Patent be granted to me for the invention or discovery described and claimed in the foregoing specification and claims, declaration, power of attorney, and this petition.

Signed at Boise, IDAHO, this 20 day of July, 1998.

Inventor: Leonard E. Mess
Leonard E. Mess
4101 Cassia
Boise, Idaho 83705

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:)
)
Leonard E. Mess)
)
Serial No.: Not Yet Assigned)
)
Filed: February 9, 2000)
)
For: SYSTEM FOR TESTING A SEMICONDUCTOR)
DEVICE)

ASSOCIATE POWER OF ATTORNEY

The Honorable Commissioner of Patents
and Trademarks
Washington, D. C. 20231

Sir:

Please recognize CHARLES L. ROBERTS, Reg. No. 32,434; DAVID L. GRIFFIN, Registration No. P-44,136; R. BURNS ISRAELSEN, Registration No. 42,685; DAVID R. TODD, Registration No. 41,348; JESÚS JUANÓS i TIMONEDA, Registration NO. 43,332; STEPHEN D. PRODNUK, Registration No. 43,020, R. PARRISH FREEMAN, Registration No. 42,556, ADRIAN J. LEE, Registration No. 42,785, and KYLE H. FLINDT, Registration No. 42,539 as associate attorneys for me in the above-entitled application. Please address all future written and telephonic communications to:

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Dated this 9 day of February 2000.

Respectfully submitted,



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